Remarks

Reconsideration of further examination is respectfully requested. Claims 1 through 11 were last presented for examination. Claims 1 through 11 were rejected. Claims 1 through 11 are submitted for further examination.

The interview with Examiner Soward on 9 October 2003 with Applicant's attorney, William W. Cochran, was greatly appreciated. In that interview, Applicant reviewed the invention with the Examiner and discussed the Hause et al. reference and Tsuchimoto references. Agreement was reached with the Examiner that neither Hause et al. or Tsuchimoto disclosed the embedding of an implantation region in the substrate, but rather, these references show low energy implantation in the epitaxial layer.

Claims 1-2, 4-7 and 9-11 were rejected under 35 USC 103(a) as being unpatentable over figure 1 of Applicant's disclosure, the Hause et al. '887 patent and the Tsuchimoto '566 patent. In the rejection, the Examiner argued that Hause teaches embedding regions in the common substrate and Tsuchimoto teaches isolation regions and masking techniques.

In addition, Examiner rejected claims 3 and 8 under 35 USC 103(a) as being unpatentable over figure 1, Hause et al. and Tsuchimoto and further in view of Diaz '445. The Examiner states in this rejection that Diaz teaches the substrate that includes an epitaxial layer 226 and underlying substrate layer 228.

Hause et al. discloses a method of making an IGFET with a selectively doped multilevel polysilicon gate. As shown in figures 1E, 1F and 1G, N-type regions 120, 122 are implanted in P-type region 106 of epitaxial layer 106, 108. P-type regions 130, 132 are implanted in N-type region 108 in the epitaxial layers 106, 108. The formation of these N and P regions in the epitaxial layers is done by low energy implantation in the epitaxial layers 106, 108. For example, see column 3, line 60 through 62 of Hause, et al. Low energy implantation is in the range of 2 to 10 KeV of the N and P regions. See column 4, line 57 of Hause, et al. As is clear from the disclosure of Hause et al., there is no implantation of an embedded region in the substrate 102 (see figure 1H) of the Hause device. See column 3, line 59 of Hause, et al.

Tsuchimoto also discloses implantation in the epitaxial layer 2 (figures 1 through 4) and epitaxial layer 31 (figures 5 through 18). See column 2, line 56, and column 3, line 50 of Tsuchimoto. Tsuchimoto also discloses low energy implantation of 50 KeV as indicated in the abstract. As is well known in the industry, 50 KeV causes the ions to be implanted in the epitaxial layer and not in the substrate. Tsuchimoto does disclose isolation between circuits, but this occurs in the epitaxial layer and not in the substrate. As disclosed in column 4, lines 13 through 15, and as shown in figures 14 through 18, the isolation regions 42 are formed in the epitaxial layer 31. Hence, there is no disclosure in Tsuchimoto of implanting ions in an embedded region of the substrate.

Applicant's claimed invention clearly distinguishes from the art of record. For example, claim 1 recites "an integrated circuit having a plurality of circuits formed on a common substrate that are isolated by isolation regions in said common substrate...." Further claim 1 recites "irradiating said common substrate with said high energy ions such that the said energy ions have an energy level sufficient to implant said high energy ions in embedded regions of said common substrate ... so that isolation regions are formed in said common substrate ... and said embedded regions are buried in said common substrate...." The other independent claims 2 and 6 include similar limitations.

Neither Hause et al. or Tsuchimoto disclose, teach or even suggest, in any manner, the implantation of ions using high energy implantation techniques to create embedded regions in the substrate. Even, assuming *arguendo*, that the references could be combined, including figure 1, the combination of such references still would not teach the embedded regions in the substrate, as set forth in Applicant's claims.

The drawings were objected to by the Examiner in that figure 1 was not labeled as prior art. As explained in the interview with the Examiner, figure 1 is not known to be part of the prior art, but constitutes an internally derived equivalent circuit that is intended to model the effects of cross-talk across the substrate. The description of figure 1 was included in the Background of the Invention to merely describe the problem solved by the present invention. As set forth in MPEP 608.01(c), one of the purposes of the Background of the Invention is to

describe the problems of the prior art and other materials. Figure 1 discloses problems associated with "other materials."

In view of the above, this application is now considered to be in condition for allowance and such action is earnestly solicited.

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Respectfully submitted,

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